REMARKS

Objection to the Drawings:

The Office Action has indicated that figures 1 to 30 should be designated as "Prior Art". Taking the Examiner's comments into consideration, figures 1, 2, 8 and 17-20 have been labeled as "Prior Art." However, figures 3-7, 9-16 and 21-30 have been labeled as "Related Art", since these figures show the problems discovered by the inventor in the prior art and which are addressed by the present invention, as discussed in the background section of the present application. Therefore, figures 3-7, 9-16 and 21-30, even though discussed in the background of the invention section of the present application, are not actually prior art, but problems discovered in the prior art.

Therefore, entry of the drawings changes in provided in the Request For Approval Of Drawing Changes provided herewith is respectfully requested. No new manner is added to the drawings. Further, withdrawal of the objection to the drawings is also respectfully requested.

Objection to the Specification:

The Office Action has indicated that on page 1, line 27, "careers" should be amended to read -- carriers --. Taking the Examiner's comments into consideration, the suggested change to the specification has been made in two places. No new manner is added to the specification. Entry of this change to the specification is respectfully requested. Withdrawal of the objection to the specification is also respectfully requested.

Objection to the Title:

The Office Action asserts that the title is not descriptive and requires that a new title be supplied. Taking the Examiner's comments into consideration, the following title is respectfully submitted.

"A Semiconductor Integrated Circuit and Fabrication Process Having Compensated Structures to Reduce Manufacturing Defects."

Entry of this change to the title is respectfully requested. Further, withdrawal of the objection to the title is also respectfully requested.

Claim Rejections under 35 USC §102

Claims 16 and 18 have been rejected under 35 USC §102(b) as being anticipated by admitted Prior Art in the applicant's specification as illustrated in Figure 8.

Figure 8 describes an integrated circuit in the prior art having a flash memory (A), a low voltage transistor (B), and mid-level voltage transistor (D), and a high voltage transistor (C). A semiconductor substrate is used as the base for each of the foregoing devices. In addition, insulation (12B) is shown with a thickness of 1.5-5 nm, insulation (12D) is shown with a thickness of 5-10 nm, and insulation (12C) has a thickness of 8-50 nm. A floating gate (13) with a control gate (16) is formed on the silicon gate (13) using an ONO film (14), as shown in figure 8B.

The present invention, as illustrated in figures 31-59 and particularly figure 47A-47D, describes a semiconductor circuit having a first through third MOS transistors in which a two layer silicon structure is used that allows the height of the gate electrode to be the same in the first through third MOS transistors.

However, the admitted prior art, as illustrated in figure 8, does not disclose or suggest stacking two silicon layers on top of each other as illustrated in figures 47A-47D. Therefore, as recited in claim 16, the first, second, and third gate electrodes have two silicon layers stacked one upon the other. Specifically, independent claim 16 recites

> "A semiconductor integrated circuit, comprising: a semiconductor substrate; a non-volatile memory formed in a memory cell region of said semiconductor substrate; a first MOS transistor formed on a first device region of said semiconductor substrate, said first MOS transistor having a first gate insulation film of first thickness and a first gate electrode; a second MOS transistor formed on a second device region of said semiconductor substrate, said second MOS transistor having a second gate oxide film of second thickness and a second gate electrode; and a third MOS transistor formed on a third device region of said semiconductor substrate, said third MOS transistor having a third gate insulation film of third thickness and a third gate electrode; said first thickness being smaller than said second thickness, said second thickness being smaller than said third thickness, said first through third gate electrodes having a substantially identical height, wherein the first, second, and third gate electrode each comprise two silicon layers stacked one upon the other. (Emphasis Added).

Therefore, the rejection of Claim 16 under 35 USC §102(b) as being anticipated by admitted Prior Art in the applicant's specification as illustrated in Figure 8 is respectfully traversed. Further, withdrawal of the rejection of Claim 16 under 35 USC §102(b) as being

anticipated by admitted Prior Art in the applicant's specification as illustrated in Figure 8 is respectfully requested.

In addition, claim 18 is allowable by virtue of its dependence on an allowable independent claim. Therefore, withdrawal of the rejection of Claim 18 under 35 USC §102(b) as being anticipated by admitted Prior Art in the applicant's specification as illustrated in Figure 8 is respectfully requested. Thus, allowance of claims 16 and 18 is respectfully requested.

Claim Rejections under 35 USC §103

Claim 17 is rejected under 35 USC §103 (a) as being unpatentable over the admitted prior art, as illustrated in figure 8, in view of Gwen et al. (U.S. patent No. 5,472,892).

Gwen et al. describes the method of the manufacturing gate memory in which a silicon layer (206) is placed in a cell array region and a silicon layer (208) is placed in a peripheral circuit region.

However, claim 17 of the present application recites that the first and third gate electrodes as having a second silicon film stacked on the first silicon film and the second gate electrodes has a second silicon film stacked on a third silicon film. Again, the admitted prior art as illustrated in figure 8 does not disclose or suggest stacking two silicon layers on top of each other as illustrated in figures 47A-47D.

Therefore, withdrawal of the rejection of claim 17 under 35 USC §103 (a) as being unpatentable over the admitted prior art, as illustrated in figure 8, in view of Gwen et al. (U.S.

patent No. 5,472,892) is respectfully requested. Further, claim 17 is allowable by virtue of its dependence upon an allowable independent claim.

Assertion of Product by Process Claims

In item 9 of the office action it is asserted that claims 17 and 18 are product by process claims. This assertion is respectfully traversed. Both claim 17 and 18 further detail the structure of the present invention as recited in claim 16. However, in order to more clearly recite the structure of the present invention, claim 17 has been amended to reflect the same. Therefore, withdrawal of the assertion that claims 17 and 18 are directed to product by process claims is respectfully requested.

CONCLUSION

It is believed that this Amendment is fully responsive to the Office Action dated **July 2, 2002**. Therefore, allowance of claims 16-18 is respectfully requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the title, specification, claims and drawings by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,
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PATENT TRADEMARK OFFICE

Enclosures: Version with markings to show changes made
Request for Approval of Drawing Corrections w/Figs. 1A-30B marked in red ink

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/960,399

IN THE DRAWINGS:

Please amend the drawings as indicated in the attached Request for Approval of Drawing Corrections.

IN THE TITLE:

Please amend the title as indicated below:

A SEMICONDUCTOR INTEGRATED CIRCUIT AND FABRICATION PROCESS [THEREOF] HAVING COMPENSATED STRUCTURES TO REDUCE MANUFACTURING DEFECTS

IN THE SPECIFICATION:

Page 1, paragraph starting at line 25, has been amended as indicated below:

In a flash memory, writing and erasing of information is done by injection and pulling out of [hot-careers] hot-carriers to or from a floating-gate electrode through a tunneling insulation film. In this operation, a high voltage is required for producing [hot-careers] hot-carriers. For this purpose, a boosting circuit is provided in a peripheral circuit that cooperates with a memory cell for boosting a power supply voltage. The transistor used in such a peripheral circuit is required to operate at high voltage.

IN THE CLAIMS:

Please amend claim 16 as follows:

16. (Amended) A semiconductor integrated circuit, comprising:

a semiconductor substrate;

a non-volatile memory formed in a memory cell region of said semiconductor substrate;

a first MOS transistor formed on a first device region of said semiconductor substrate, said first MOS transistor having a first gate insulation film of first thickness and a first gate electrode;

a second MOS transistor formed on a second device region of said semiconductor substrate, said second MOS transistor having a second gate oxide film of second thickness and a second gate electrode; and

a third MOS transistor formed on a third device region of said semiconductor substrate, said third MOS transistor having a third gate insulation film of third thickness and a third gate electrode;

said first thickness being smaller than said second thickness, said second thickness being smaller than said third thickness,

said first through third gate electrodes having a substantially identical height, wherein the first, second, and third gate electrode each comprise two silicon layers stacked one upon the other.

17. (Amended) A semiconductor integrated circuit as claimed in claim 16, wherein said first and third gate electrodes have a structure in which a second silicon film is stacked on a first

silicon film, said second gate electrode has a structure in which said second silicon film is stacked on a third silicon film, and wherein said non-volatile memory is formed of a floating gate electrode formed of said third silicon film and a control gate electrode formed on said floating gate electrode via an insulation film and having a structure in which said first silicon film and said second silicon film are consecutively stacked [consecutively].